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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/829,136	04/09/2001	Frankie F. Roohparvar	400.017US01	7233

27073 7590 07/29/2004

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/829,136	ROOHPARVAR, FRANKIE F.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-41 are presented for examination.

Drawings

The drawings were received on June 1, 2004. These drawings are acceptable.

Response to Arguments

Applicant's arguments filed June 1, 2004 have been fully considered but they are not persuasive.

The following 35 U.S.C. 112 rejections are maintained as specified below.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 34-41 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Independent claims 34, 38 and 41 recite variables, which are not defined.

As per claim 34, it is unclear to the examiner if the "X" in "X-data" line 4, and "X-control" lines 6 and 7 are the same "X". It is also unclear where the "X/Y" recited in line 7 is described or defined. It is also not clear if the "X" in "X-data", "X- control", and "X/Y" are related in any way or if they are the same.

As per claims 38, and 41, the same issue exists for "X/Y" in line 3 of both claims and "X-bits" in line 2 of both claims. "X/Y" is not defined and "X" is not defined. It is also not clear if the "X" in "X-bits", and "X/Y" are related in any way or if they are the same.

Dependent claims 35-37 and 39-40 inherit the 35 U.S.C. 112, first paragraph issues of the independent claims and will not be further examined on the merits.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 28-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 28, the term "X" is not defined in the claim, such as "where x is a positive integer greater than 1"

Claims 29-33 inherit the 35 U.S.C. 112, second paragraph issues if the independent claim and may not be further examined on the merits.

Claims 20-24, 27, and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 20, in line 5 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode.

As per claim 22, in line 5 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode.

As per claim 23, this claim is dependent on claim 22 and inherits the 35 U.S.C. 112, second paragraph issues of the independent claim.

As per claim 27, in line 5 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode. In lines 7 and 8 the phrase "a high voltage signal is detected on a predetermined address input" is unclear to the examiner as there is no stated relation of the testing with the address input within the claims. In line 9, "the address inputs" is unclear due to the plural form of the word inputs where above in the claim only a predetermined address input is mentioned.

As per claim 32, in line 5 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode.

As per claim 33, this claim is dependent on claim 32 and inherits the 35 U.S.C. 112, second paragraph issues of the independent claim.

As per claim 38, in line 7 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode.

As per claim 39, this claim is dependent on claim 38 and inherits the 35 U.S.C. 112, second paragraph issues of the independent claim.

As per claim 41, in line 7 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode.

Applicant's arguments on the matter of the high voltage signal, see below, filed June 1, 2004, with respect to claims 21, 24 and 40 have been fully considered and are persuasive. The 35 U.S.C. 112 rejection of claims 21, 24 and 40 has been withdrawn.

"Applicant respectfully submits that the phrase "a high voltage signal is detected on a pre-determined address input" refers to the memory device detecting an elevated voltage from that of a normal signal level on a selected address input. Applicant refers to the paragraph starting on line 15, page 11 of the Specification, which further states in part,"[f]or example, an elevated voltage must be provided on a pre-selected address input connection to initiate a test mode. Thus, a voltage detection circuit 190 monitors the address input. Once an elevated voltage is detected, the test mode is entered and a selected test can be specified."

Claim Rejections - 35 USC § 102

As per claims 1 and 7, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a non-volatile memory device that initiates a test mode selected by test codes received on the address inputs) are not recited in the rejected claim 1. Test codes are not mentioned in claim 1. The phrase "test codes received on the address inputs" is not included in this claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

As per claims 7, 13, 16, 22, 25 and 27, Applicant stresses that the test codes are provided on the address. However the prior arts cited teach '*appropriate test mode codes are placed on the I/O lines'* Roohparvar (see below) and '*The test mode utilizes the existing read data path of the flash memory device. During the test mode, the user places an address and a test voltage on inputs to the device. This test voltage is routed directly to the gates of the flash memory transistors selected by the address.*' Akaogi et al. (see below). As the prior arts do not limit which input or I/O is being used the prior art rejection is maintained.

Roohparvar teaches the claimed circuit for generating test-mode signals for memory which uses both hardware and software protection schemes. The circuit enters a test code by receiving a high voltage at two terminals. The high voltage must remain

on at least one of the terminals during the test code process. Otherwise, the circuit is reset. The test code contains test code bits and format code bits. The format code bits are the same for all test codes and distinguish the test codes from commands. (abstract) *A high voltage is placed on two or more pins in order to initiate the test mode.* The high voltage is detected by detectors, which may be implemented with known detector circuits. Then, the CE signal is brought low and *appropriate test mode codes are placed on the I/O lines and into the buffer.* The AND gate ensures that both inputs have a high voltage in order initiate the test code process. The output of the AND gate and the CE signal form the inputs to AND gate. Therefore, with both inputs HIGH, one input will be HIGH. When the other input (CE) is also HIGH, the output is HIGH and turns on transistor, which functions as a switch to transfer the I/O signal from the buffer to a test mode code latch. On the high going edge of the CE signal, the test mode code is latched into a test mode code latch. Since two or more pins must be at high voltage at the same time during the code entry, this affords the hardware protection during entry of the test code. Therefore, two pins are at a high voltage to load the test mode code and then one of the pins is brought to a low voltage to shut off the loading. If WE falls below the second predetermined voltage, latch is reset through the inverter, disabling the test mode. (Figure 1, column 3 lines 7-42)

Akaogi et al. teach that the flash memory transistor to be tested is selected by placing its address on the address inputs of the device. If the voltage placed on the gate is greater than the Vt of the selected transistors, the device, will output a logical 1 for the corresponding bit location otherwise it will output a logical 0. Changing the input

address to the device tests each transistor. The test mode utilizes the existing read data path of the flash memory device. During the test mode, the user places an address and a test voltage on inputs to the device. This test voltage is routed directly to the gates of the flash memory transistors selected by the address. (Column 4 lines 1-15, column 13 lines 7-50, figure 2)

As per claims 28 and 29, applicant states that the cited reference does not disclose testing a memory device. However, Fang et al. teach "The ROM read-out device 40 is used for reading the program code from the application program memory 34 to test whether the application program memory 34 can be read properly, so that the application program stored therein can be executed properly." (Column 3 lines 21-26) Therefore the reference does teach testing of a memory. The rejection is maintained.

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Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CB

Cynthia Britt
Examiner
Art Unit 2133

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